REMARKS

The Final Office Action mailed April 9, 2002, has been received and reviewed.

Claims 1 through 11, 13, 16 through 25, 51 through 61, 63, 66 through 75 are currently under examination in the application, of which claims 1 and 51 are independent. Claims 1 through 11, 13, 16 through 25, 51 through 61, 63, 66 through 75 stand rejected. Applicant respectfully traverses the rejection of such claims, as hereinafter set forth.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. 6-151492 to Sony Corporation in view of U.S. Patent No. 6,081,997 to Chia et al.

Claims 1 through 11, 13, 16 through 21, 24, 25, 51 through 61, 63, 66 through 71, 74, and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sony Corporation (Japanese Patent No. 6-151492) in view of Chia et al. (U.S. Patent No. 6,081,997). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

In the rejection, the Examiner acknowledges that the Sony reference is deficient by stating: "Sony does not have at least a portion of at least one cavity covering bond pads of the structures." The Examiner relies on the Chia reference to overcome such deficiency by suggesting that the Chia reference teaches the semiconductor substrate having conductive

structures on both the underside surface and upper surface. In particular, the Examiner suggests that the Abstract references "protruding conductive structures on both sides, the underside and upper surface," and then further suggests that "molding 26 shields the [upper] surface and its conductive structure from the flowable resin." (Office Action, page 3, lines 13-15; page 5, lines 16-20).

Applicant respectfully disagrees with the Examiner's rejection for at least three reasons. First, the Examiner's reference to the Abstract of the Chia reference of teaching conductive structures on the upper surface of the semiconductor substrate is incorrect; second, the Sony reference and the Chia reference, alone and in combination, do not teach or suggest each and every claim limitation of the claimed invention; and, third, a person of ordinary skill in the art would not have been motivated to modify the references to overcome the references' deficiencies with respect to the claimed invention.

Turning to the first issue, the Examiner's reference to the Abstract of the Chia reference of teaching "conductive structures on . . . the upper surface" of the semiconductor substrate is incorrect. Rather, Chia's Abstract teaches I/O pads on an under side of an integrated circuit chip 12 and bonding pads on an upper surface of a substrate 14,which is formed of a printed circuit board material (Chia, Col. 5, lines 58-63) and is <u>not</u> a semiconductor substrate. Specifically, the Abstract in the Chia reference states the following:

> A system and method are presented for forming a grid array device package around an integrated circuit. The integrated circuit includes multiple I/O pads on an under side surface, and <u>an upper surface of a substrate</u> includes a corresponding set of bonding pads. The <u>substrate also has an opening</u> (i.e., a hole) extending therethrough and preferably substantially in the center of the set of bonding pads (emphasis added). . . .
> Chia, Abstract.

As clearly shown, the substrate referenced in the Abstract which includes bonding pads on the upper surface thereof is substrate 14. The bonding pads on the upper surface of the substrate are interconnected to the solder bumps 16 and are spaced away from mold section 26 by the thickness of substrate 14. None of the solder bumps 16, bonding pads and I/O pad "abut" the

inner surface of the mold section 26 or any other mold surface. *See* Chia, col. 5, line 30 - col. 6, line 52; FIGS. 1-3.

Examiner's section on page 5 in the Office Action entitled "Response to Arguments", it appears that the Examiner's reasons for finding Applicant's arguments submitted 4 January 2002 unpersuasive is on the premise that Chia's Abstract teaches the "semiconductor substrate 12 of figs. 1-3 to having protruding conductive structures on both sides, the underside and upper surface, . . ." As previously set forth, Applicant respectfully submits that this premise is incorrect. Rather, the Abstract states that semiconductor substrate 12 includes I/O pads on its underside surface and that substrate 14 includes bonding pads on its upper surface, as previously set forth in detail. Thus, the Chia reference does not overcome the deficiencies of the Sony reference. Applicant therefore respectfully traverses this rejection and respectfully requests the Examiner reconsider and withdraw the rejection of claims 1-11, 13, 16-21, 24, 25, 51-61, 63, 66-71, 74, and 75 under 35 U.S.C. § 103(a) based on the Sony reference and the Chia reference.

Turning to the second issue, the Sony reference and the Chia reference, alone and in combination, do not teach or suggest each and every claim limitation of the claimed invention. In the Sony reference, there is disclosed a first and second mold 1 and 2 opposing each other which forms a cavity 13 therebetween. A lead frame 5 with a semiconductor chip 15 mounted thereon is held in the cavity 13 which is oriented vertically. A resin 16 is then injected in the cavity at an underside thereof so that the resin 12 fills the cavity from the bottom to the top thereof. *See* Sony reference, Abstract and FIGS. 7-10.

The Chia reference discloses a semiconductor assembly including a chip 12 mounted face down to a substrate 14 in a flip-chip type arrangement. The substrate 14 includes an opening 18 extending therethrough in a center location of the substrate 14. The assembly is placed in a mold having a first mold section 20 and a second mold section 26, wherein the first mold section 10 includes a mold opening 22 which is made to correspond with the opening 18 in the substrate 14. The assembly is therefore placed on the first mold section 20 with the opening 18 in the substrate 14 corresponding with the mold opening 22 of the first mold section 26. The second mold

section is then placed over and against the back face of the chip 12. An encapsulant 32 is provided by pressurized injection through the openings 22 and 18 and then in the gap between the chip 12 and substrate 14 and to the periphery of the assembly. *See* Chia, col. 5, line 30 - col. 6, line 52; FIGS. 1-3.

Turning to independent claim 1, neither the Sony reference nor the Chia reference teach or suggest "positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate; . . . (emphasis added)" As previously discussed, the Sony reference discloses the inner surface of the mold as being separate from the chip since the Sony reference discloses a lead frame type assembly. The Chia reference teaches the second mold section 26 as abutting with the back surface of the chip 12, but the first mold section 20 is not positioned with "portions" abutting the conductive elements of the chip. Rather, the Chia reference discloses the first mold section abutting with the substrate 14.

Thus, the Sony reference and the Chia reference, alone and in combination, does not teach or suggest each and every limitation of claim 1, namely, the deficiency of "portions" of the inner surface of a mold abutting conductive elements on a semiconductor substrate.

With respect to the third issue, a person of ordinary skill in the art would not have been motivated to modify the references to overcome the references' deficiencies with respect to the claimed invention. In particular, there is nothing taught or suggested in both the Sony reference and the Chia reference regarding "positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate," as recited in claim 1. Thus, since such claim limitation is neither taught or suggested in the Sony reference and the Chia reference, there

would have been no motivation for a person of ordinary skill in the art to modify the methods disclosed in the references to overcome such deficiency.

In addition, independent claim 51 recites similar claim recitations to those of claim 1 and, therefore, claim 51 should be patentably distinguishable over the Sony reference and the Chia reference for at least the same reasons as independent claim 1. With respect to dependent claims 2-11, 13, 16-21, 24-25, 52-61, 63, 66-71 and 74-75, they are patentable over the Sony reference and the Chia reference based on at least their respective dependencies from claims 1 and 51.

Furthermore, dependent claims 24, 25, 74 and 75 are patentable over the Sony reference and the Chia reference in light of further limitations recited therein. Turning first to claims 24 and 74, the Sony reference and the Chia reference do not teach or suggest "portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate," as recited in claims 24 and 74. Rather, the inner surface in the mold of the Sony reference is separated from the semiconductor chip by a gap of encapsulation material. The Chia reference discloses that the portion of the transfer mold in contact with the semiconductor chip is a flat surface and further, the transfer mold does not contact any of the conductive elements on the semiconductor chip. Thus, claims 24 and 74 are patentably distinguishable over the Sony reference and the Chia reference, alone and in combination, in light of further limitations recited therein.

With respect to claims 25 and 75, the Sony reference and the Chia reference do not teach or suggest "wherein said providing said at least one substrate comprises providing said at least one substrate having said at least one surface with conductive structures protruding therefrom, and wherein said providing said transfer mold comprises configuring each portion of said portions of said inner surface of said transfer mold to comprise a recess to at least partially receive a corresponding one of said conductive structures so that said flowable material partially covers said conductive structures," as recited in claims 25 and 75. Rather, the Chia reference discloses that the portion of the transfer mold in contact with the semiconductor chip is a flat surface (not a recess) and further, the transfer mold does not contact any of the conductive

structures protruding from the semiconductor chip. As before, the Sony reference discloses that the inner surface in the mold is separated from the semiconductor chip by a gap of encapsulation material. Thus, claims 25 and 75 are patentably distinguishable over the Sony reference and the Chia reference, alone and in combination, for further reasons recited therein.

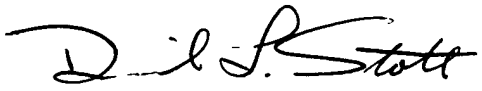
Obviousness Rejection Based on Japanese Patent No. 6-151492 to Sony Corporation in view of U.S. Patent No. 6,081,997 to Chia et al., and further in view of U.S. Patent No. 5,471,369 to Honda et al.

Claims 22, 23, 72, and 73 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sony Corporation (Japanese Patent No. 6-151492) in view of Chia et al. (U.S. Patent No. 6,081,997), and further in view of Honda et al. (5,471,369). However, as set forth above, independent claims 1 and 51 are patentably distinguishable over the Sony reference and the Chia reference. Furthermore, the Honda reference does not overcome the deficiencies in the Sony reference and the Chia reference of "positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate," as recited in claims 1 and 51. Therefore, claims 22, 23, 72, and 73 are patentable over the Sony reference, the Chia reference and the Honda reference based on at least their respective dependencies from claims 1 and 51.

CONCLUSION

Claims 1 through 11, 13, 16 through 25, 51 through 61, 63, 66 through 75 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,



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